23. (Amended) A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

D3

forming a nitrogen doped region in said source and drain regions by nitrogen implantation; and

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electron injection into said gate electrode.

REMARKS

Rejections under Double Patenting

In the Final Office Action, the Examiner rejected Claims 1-15 and 23-28 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-8 of U.S. Patent No. 5,405,791. Applicant respectfully traverses the rejections and submits that the pending claims in the present application are patentably distinct from the claims of U.S. Patent No. 5,405,791 ("Ahmad").

The claims of the Ahmad patent reflect the disclosure of Ahmad, which is distinguished below. In particular, the claims of Ahmad relate to forming disposable spacers, by deposition, and implanting ***conductivity-enhancing dopants***, not to "transforming" a portion of the gate conductor, nor to implanting "insulator elements" in the substrate.

Accordingly, Applicant respectfully requests withdrawal of the rejections for obviousness-type double patenting.

Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-15 and 23-28 under 35 U.S.C. § 103(a) as being unpatentable over Ahmad et al. (U.S. Patent No. 5,405,791) in view of Wu et al. (U.S. Patent No. 5,837,585). Ahmad et al. taught forming an insulator region on the substrate (a silicon nitride etch stop layer) and also taught implanting conductive dopants, arsenic or boron. Wu taught implanting nitrogen into a silicon oxide dielectric layer. Accordingly, the Examiner states that "it would have been obvious to one or ordinary skill in the art at the time of the invention to substitute Ahmad's Arsenic with Wu's Nitrogen in Ahmad's process to form an oxide layer with very high electron injection efficiency and very large charge-to-breakdown voltage."

In telephonic interviews with the Examiner, the Examiner indicated that Ahmad et al. discloses all of the steps, albeit in a very different sequence than that claimed, but that a prima facie case of obviousness had been made.

Applicant respectfully traverses the finding and submits that a *prima facie* case of obviousness must include a suggestion for the asserted combination. "Before the PTO may combine the disclosures of two or more prior art references in order to establish ***prima facie*** obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." *In re* Jones, 21 U.S.P.Q.2d 1941, 1943-44 (Fed. Cir. 1992) (emphasis added).

Furthermore, a *prima facie* case of obviousness must also include the reasonable expectation of success. "Both the suggestion [to combine] and the ***expectation of success***, must be founded in the prior art, not in the applicant's disclosure." *In re* Dow Chemical Co., 5 U.S.P.Q.2d 1529, 1530 (Fed. Cir. 1988) (emphasis added).

In the present case, not only would the skilled artisan not have expected success, but the asserted combination would have ***destroyed*** the Ahmad et al. reference. In particular, substitution of nitrogen for the implanted arsenic or boron of Ahmad et al., as asserted in the Examiner's rejections, would have resulted in a non-functional device. As the skilled artisan will readily appreciate, arsenic and boron are ***conductivity-enhancing*** elements that are necessary for electrical operation of the transistors being formed in the process of Ahmad et al. Nitrogen could not serve this function.

Ahmad taught "a boron halo implant which creates N-channel anti-punchthrough regions 61, and low dosage arsenic source/drain implant which creates lightly-doped N-channel source/drain regions 62." (Col. 4, ln. 29-33) The skilled artisan would understand that the purpose of these dopings was to tailor the conductivity of transistor structures.

Wu taught nitrogen to nitridize a thin tunnel oxide, and thus improved the flash memory cell formed therefrom.

Accordingly, the skilled artisan would not have been motivated to employ the nitrogen implantation of Wu, whose purpose was to increase performance of flash memory cell tunnel oxides, for the arsenic and boron doping of Ahmad, whose purpose was to increase conductivity of transistor structures in the substrate. There is no suggestion or motivation to combine these references. Whereas arsenic and boron increase the conductivity of silicon, nitrogen makes silicon

less conductive. In fact, using the nitrogen implantation of Wu in place of arsenic and boron in the transistor of Ahmad would render Ahmad inoperative.

Dependent Claims 2-12, 14 and 24-28 each depend from one of these independent claims and therefore include all the features and limitations thereof. Furthermore, the dependent claims add further distinguishing features of particular utility. Accordingly, Applicants submit that the dependent claims are also allowable over the art of record.

CONCLUSIONS

In view of the foregoing remarks, Applicant respectfully requests reconsideration of the claims and submits that the application is in condition for allowance. If, however, some issue remains which the Examiner feels may be addressed by Examiner's amendment, the Examiner is cordially invited to call the undersigned for authorization.

Respectfully submitted,
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: July 18, 2001

By: Adeel Syed Akhtar

Adeel S. Akhtar
Registration No. 41,394
Attorney of Record
620 Newport Center Drive, Sixteenth Floor
Newport Beach, CA 92660
(415) 954-4114

W:\DOCS\ASA\ASA-9591.DOC
071701

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 2 has been cancelled.

1. (Twice Amended) A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

~~forming~~ implanting an insulator element region ~~on~~ into said substrate; and

transforming a portion of said conductive layer adjacent said insulator element region into a sidewall spacer after forming the insulator element region.

3. (Amended) The process of Claim 1, wherein said ~~insulator element region~~ substrate comprises ~~said insulator element and~~ silicon.

23. (Amended) A process of eliminating hot electron injection into a gate electrode positioned on a gate oxide adjacent a channel interposed between a source and a drain region in a silicon substrate, the process comprising:

forming a nitrogen doped region in said source and drain regions by nitrogen implantation; and

forming a silicon nitride film over a portion of said gate electrode so that a portion of said silicon nitride film penetrates under said gate electrode during said forming step wherein said portion of said silicon nitride film prevents hot electron injection into said gate electrode.

W:\DOCS\ASA\ASA-9591.DOC
071701